REMARKS

Status of the Claims

- Claims 1, 9-13, 20-22, and 25-29 are pending in the Application after entry of this amendment.
- Claims 1, 3-22, 24-29 are rejected by Examiner.
- Claims 1, 13, 20-22, and 28 are amended by Applicant.
- Claims 3-7, 14-19, and 24 are newly cancelled by Applicant.

Response to Argument

Page 2 item #1 of the Office Action dated 5/3/06 indicates that the Examiner interprets the term "complex graphic" to include a bitmap as taught by Koselj. Applicant has amended independent Claims 1, 13, 22, and 26 to recite exemplary forms of complex graphic that do not include a bitmap. These complex graphic forms are supported by at least paragraph 0035 in the originally filed specification of the present Application. Applicant submits that the enumerated forms of complex graphic more clearly define that which Applicant defines as his invention.

Claim Rejections Pursuant to 35 U.S.C. §102

Claims 1, 3-7, 9, 11-19, 21, 22, 24 and 26-28 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 2003/0214506 to Koselj et al. Applicant respectfully traverses the rejection.

Applicant has amended independent Claims 1, 13, 22, and 28 to include that a complex graphic including at least one of shading, texturing, alpha-blending, anti-aliasing, and sub-pixel manipulation. This is in addition to the aspect that rendering the complex graphic is performed in the system random access memory with the central processing unit wherein the graphical processing unit is bypassed. Applicant has cancelled Claims 3-7, 14-19, and 24 because their content is incorporated into their respective independent claims.

Koselj et al. discloses that:

> "For the first time, the inventors have realised that a graphics engine need not be provided in the CPU part of a device, but may be held in the display module. They have been able to design a hardware *graphics engine that is sufficiently simple that it can be embedded in a display driver IC for a small-area display or in a display module for a portable electrical device*. Since the *graphics engine is in the display module*, high-level graphics commands travel between the CPU and the display part of the mobile device, rather than pixel data. Use of graphics engines as opposed to non-accelerated CPU processing reduces power consumption. Use of the graphics engine in the display module allows considerable savings in power in a device of almost identical size and weight." (paragraph 0020).

Applicant submits that the hardware graphics engine taught by Koselj is a driver integrated circuit (IC) that is not part of, and is removed from, the CPU because it is embedded in a display driver IC. Even though high level graphics commands travel between the CPU and the display part of a mobile device, the display driver IC itself is the hardware graphics engine, not the CPU.

Page 3 of the Office Action dated 5/3/6 indicates that the Koselj teaches sub-pixel manipulation and anti-aliasing at paragraph 0026 of Koselj, complex graphic shading at paragraph 0129, and alpha-blending at paragraph 0032. Applicant respectfully traverses that Koselj teaches these forms of complex graphics are rendered in system memory by the CPU instead of the graphical processing unit as recited in the independent Claims 1, 13, 22, and 28.

Koselj at paragraph 0025 teaches:

> "In preferred embodiments, *the graphics engine includes edge drawing logic/circuitry linked to an edge buffer* (of finite resolution) to store spatial information for (the edges of) any polygon read into the engine. This logic and edge buffer arrangement not only makes it possible to discard the original data for each edge once it has been read into the buffer, in contrast to the previous software engine." (paragraph 0025).

Thus, Applicant submits that the graphic engine comprises an edge buffer that is in the driver IC and not the CPU.

Koselj at paragraph 0026 teaches:

> "*The edge buffer* may be of higher resolution than the front buffer of the display memory. For example, the edge buffer may be arranged to store sub-pixels, a plurality of sub-pixels corresponding to a single display pixel. The sub-pixels preferably switch between the set and unset states to store the spatial information. The provision of sub-pixels (more than one for each corresponding pixel of the display) facilitates

> manipulation of the data and anti-aliasing in an expanded spatial form, before consolidation into the display size. The number of sub-pixels per corresponding display pixel determines the degree of anti-aliasing available. Use of unset and set states only mean that the edge buffer requires one bit of memory per sub-pixel." (paragraph 0026).

Applicant submits that since the edge buffer of the graphics engine IC is used to store sub-pixels and this facilitates manipulation, the sub-pixel manipulation is performed in the graphics engine IC, not the CPU. Therefore, paragraph 0026 does not teach that sub-pixel manipulation is rendered in system memory by the CPU instead of the graphical processing unit as recited in the independent Claims 1, 13, 22, and 28.

Koselj at paragraph 0029 teaches:

"*The graphics engine preferably includes a back buffer* to store part or all of an image before transfer to a front buffer of the display driver memory. Use of a back buffer avoids rendering directly to the front buffer and can prevent flicker in the display image." (paragraph 0029).

Koselj at paragraph 0032 teaches:

> "Advantageously, *the colour of each pixel stored in the back buffer* is determined in dependence on the colour of the pixel in the polygon being processed, the percentage of the pixel covered by the polygon and the colour already present in the corresponding pixel in the back buffer. This colour-blending step is suitable for anti-aliasing."(paragraph 0032).

Applicant submits that since the back buffer, located in the graphics engine IC, is advantageously used to store the colour of each pixel, then alpha-blending is conducted from the graphics engine IC, not the CPU. Therefore, paragraph 0032 does not teach that complex graphics comprising alpha-blending is performed by the CPU instead of the graphical processing unit as recited in the independent Claims 1, 13, 22, and 28.

Koselj at paragraph 0129 teaches:

> "The resolution of the polygon in the back buffer is one quarter of its size in the edge buffer in this example. The benefit of the two-pass method and amalgamation before storage of the polygon in the back buffer is that the total amount of memory required is significantly reduced. The edge buffer requires 1 bit per sub-pixel for the set and unset values. *However, the back buffer requires 16 bits per pixel to represent the shade* to be displayed and, if the back buffer were used to set boundary sub-pixels and fill the resultant polygons, the amount of memory required would be eight times

greater than the combination of the edge and back buffers, that is, sixteen 16 bit buffers would be required, rather than two." (paragraph 0129).

Applicant submits that since the back buffer, located in the graphics engine IC, uses 16 bits to represent shade, then shading is handled in the graphics engine IC, not the CPU. Therefore, paragraph 0129 does not teach that complex graphics comprising shading is performed by the CPU instead of the graphical processing unit as recited in the independent Claims 1, 13, 22, and 28.

Applicant submits that Koselj does not teach all the elements of amended independent Claims 1, 13, 22, and 28. Koselj fails to teach rendering a complex graphic in the system random access memory with the central processing unit, bypassing the graphical processing unit, wherein the complex graphic includes at least one of shading, texturing, alpha-blending, anti-aliasing, and sub-pixel manipulation.

Applicant further submits that Koselj specifically teaches that the rendering of complex graphics, as recited in the amended independent claims, is performed in a graphics engine IC apart from the CPU. Hence, Koselj teaches away from a rendering of a complex graphic in the system random access memory with the central processing unit, bypassing the graphical processing unit, wherein the complex graphic includes at least one of shading, texturing, alpha-blending, anti-aliasing, and sub-pixel manipulation as recited in the amended independent claims because Koselj requires the complex graphics to be rendered via a separate graphics engine IC located in a display. Accordingly, Koselj cannot anticipate amended Claims 1, 13, 22 and 28 and their respective pending dependent Claims 9, 11-13, 21, 24 and 26, 27 and 29 because not all elements can be found in Koselj. Applicant respectfully requests withdraw of the 35 USC §102(e) rejection of Claims 1, 9, 11-13, 21, 22, and 26-28 as these claims now patentably define over the cited art.

Claim Rejections Pursuant to 35 U.S.C. §103

Claims 10, 20, 25 and 29 stand rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent Application Publication No. 2003/0214506 to Koselj et al. in view of U.S. Patent Application Publication No. 2002/0196256 to Hoppe et al. Applicant respectfully traverses the rejection.

Applicant notes that Claims 10, 20, 25 and 29 depend on amended Claims 1, 13, 23 and 28 respectively. Claims 1, 13, 22, and 28 patentably define over Koselj et al. as stated above.

Koselj et al. teaches a display driver integrated circuit including a hardware-implemented graphics engine that teaches away from amended independent Claims 1, 13, 23 and 28 as discussed above.

Hoppe et al. teaches a system and method to effect the reduction of aliasing artifacts along discontinuity edges of a rendered polygon mesh by overdrawing the edges as antialiased lines. The processes of Hoppe et al. are targeted to be effective at reducing the temporal artifact known as "crawling jaggies". (Hoppe et al., Abstract)

Hoppe teaches in a conclusion paragraph at 0092:

> "Described above is an edge overdraw technique that reduces discontinuity edge artifacts. For typical models having a small proportion of discontinuity edges, edge overdraw can be performed with little added cost. While the method is designed for spatial antialiasing, it reduces the "crawling jaggies" artifact." (paragraph 0092).

The effect of Hoppe is to reduce crawling jaggies (see also 0020). Hoppe teaches in paragraph 0024 that "FIG. 2 is a block diagram of an exemplary graphics computing device that implements a discontinuity edge overdraw process for reducing the crawling jaggies." (0024). Referring to Figure 2, Applicant notes that the GPU 206 contains the renderer 240 and the overdrawer 242 that is useful in reducing the crawling jaggies.

Paragraph 0040 of Hoppe teaches:

> "The GPU 206 includes a rendering module 240 and an overdrawing module 242, which can be implemented in hardware or a combination of hardware and software. The rendering module 240 renders the triangles from the mesh 232 and places the rendered images in the frame buffer 208." (paragraph 0040).

Since rendering is performed in the GPU 206 and not the CPU 202 of Hoppe, Applicant submits that Hoppe, like Koselj, also teaches away from the pending independent claims which recite rendering a complex graphic in system random access memory with the CPU as recited in the amended claims. Thus, there is no motivation to combine Hoppe with Koselj in constructing a 35 USC §103 rejection of the pending claims because both fail to teach rendering complex graphics with a central processing unit instead of a separate graphics processing unit as recited in the pending claims. Applicant also respectfully submits, that

even if Koselj and Hoppe were combined, their combination still teaches away from the amended claims.

Thus, Applicant respectfully submits that neither Koselj et al. nor Hoppe et al., either considered individually or in combination, teach rendering a complex graphic in the system random access memory with the central processing unit where the complex graphic includes at least one of shading, texturing, alpha-blending, anti-aliasing, and sub-pixel manipulation; and copying said complex graphic from the system random access memory directly into the frame buffer by the central processing unit, wherein copying directly into the frame buffer bypasses the graphical processing unit as recited in amended independent Claims 1, 13, 22, and 28.

Further, Applicant notes that there is no motivation to combine Koselj with Hoppe because both teach away from the combined elements of the recited claims. Thus the combination of Koselj et al. and Hoppe et al. cannot render obvious Claims 10, 20, 25 and 29 because these claims depend on amended independent Claims 1, 13, 22, and 28 respectively which patentably define over the cited art. Applicant respectfully requests withdrawal of the §103(a) rejection.

Conclusion

In view of the above amendments and remarks, Applicant submits that the present application is in a condition for allowance upon entry of the amendments herein. Applicant respectfully and earnestly solicits a Notice of Allowance for all pending claims.

Respectfully submitted,

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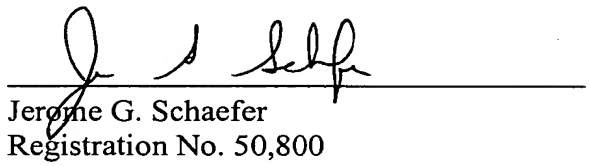

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